IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Yeo, *et al.*	Docket No.:	TSM03-0511
Filed:	Herewith	Examiner:	TBD
Serial No.:	TBD	Art Unit:	TBD
For:	Multiple-Gate Transistors Formed on Bulk Substrates		

Mail Stop: Patent Application
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

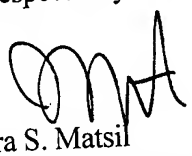
Dear Sir:

Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08A that may be considered material to the examination of the above-identified application.

Pursuant to 37 CFR 1.98(a)(2)(i), as amended, copies of U.S. Patents cited are not being submitted. However, Applicant has included copies of the non-patent literature.

No fee is due at this time, as this Information Disclosure Statement is being filed concurrently with the patent application.

Respectfully submitted,



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September 24, 2003
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PTO/SB/08A (05-03)
Approved for use through 05/31/2003. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	TBD
Filing Date	Herewith
First Named Inventor	Yeo, *et al.*
Art Unit	TBD
Examiner Name	TBD
Attorney Docket Number	TSM03-0511

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	A	US-6,252,284 B1	06-26-2001	Muller, *et al.*	
	B	US-6,391,695 B1	05-21-2002	Yu	
	C	US-6,391,782 B1	05-21,2002	Yu	
	D	US-6,413,802 B1	07-02-2002	Hu, *et al.*	
	E	US-6,432,829 B1	08-13-2002	Muller, *et al.*	
	F	US-6,451,656 B1	09-17-2002	Yu, *et al.*	
	G	US-6,492,212 B1	12-10-2002	leong, *et al.*	
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3] - Number[4] - Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, *magazine*, *journal*, *serial*, *symposium*, *catalog*, etc.), date, *page(s)*, *volume-issue* number(s), publisher, city and/or country where published.	T[2]
	H	HUANG, X., et al. "Sub-50 nm P-Channel FinFET," IEEE Transactions on Electron Devices, Vol. 48, No. 5 (May 2001) pp. 880-886.	
	I	YANG, F.L., *et al.* "35nm CMOS FinFETs," 2002 Symposium on VLSI Technology Digest of Technical Papers, (June 2002) pp. 109-110.	
	J	WONG, H.-S.P. "Beyond the Conventional Transistor," IBM Journal of Research and Development (March/May 2002) pp. 133-167.	
	K	CHAU, R., *et al.* "Advanced Depleted-Substrate Transistors: Single-gate, Double-gate and Tri-gate," Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, (2002) pp. 68-69.	
	L	YANG, F.L., *et al.* "25nm CMOS Omega FETs," International Electron Devices Meeting, Digest of Technical Papers, (December 2002) pp. 255-258.	
	M	COLINGE, J.P., *et al.* "Silicon-on-Insulator "Gate -All-Around Device"," International Electron Devices Meeting, (1990) pp. 595-598.	
	N	LEOBANDUNG, E. "Wire-Channel and wrap-around-gate metal-oxide-semiconductor field-effect transistors with a significant reduction of short channel effects," Journal of Vacuum Science and Technology, Vol. B15, No. 6, (November/December 1997) pp. 2791-2794.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.